

Serial Number 10/749,564

### AMENDMENTS TO CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Original) A video system for flat panel display having a frame buffer comprising:
  - a pre-frame-buffer processor receiving video signals, decoding and deinterlacing the video signals, and providing motion information;
  - a frame buffer controller for providing one or a plurality of field delay to the video signals output from the pre-frame-buffer processor;
  - a scaler receiving the video signals output from the pre-frame-buffer processor directly or from the frame buffer controller, and converting sample rate of the signals according to the feature of the flat panel display; and
  - a de-motion-blur processor receiving the video signals from the frame buffer controller and scaler, receiving the motion information from the pre-frame-buffer processor, comparing current video signals and previous video signals from the frame buffer controller to obtain a temporal difference, and performing over driving for the flat panel display according to the motion information and the temporal difference.
2. (Original) The system as claimed in Claim 1, wherein the motion information comprises at least a motion and noise indication signal.
3. (Original) The system as claimed in Claim 1, wherein the motion information comprises at least a film mode indication signal, which is used to enable or disable the over driving.

**Serial Number 10/749,564**

4. (Original) The system as claimed in Claim 1, wherein said pre-frame buffer processor comprises a color TV decoder for decoding the video signals and providing motion information to the de-motion-blur processor.

5. (Original) The system as claimed in Claim 4, wherein said color TV decoder has an access to the frame buffer controller providing one or a plurality of field delays for the operation of the color TV decoder.

6. (Original) The system as claimed in Claim 1, wherein said pre-frame buffer processor comprises a video source selector for selecting the source of the video signal.

7. (Original) The system as claimed in Claim 1, wherein said pre-frame buffer processor comprises a pre-scaler video processing unit for performing at least one of features of color transient improvement, luminance transient improvement, noise reduction, and flesh tone adjustment.

8. (Original) The system as claimed in Claim 1, wherein said pre-frame buffer processor has an access to the frame buffer controller providing field delay for noise reduction.

9. (Original) The system as claimed in Claim 1, wherein said pre-frame buffer processor comprises a deinterlacer for performing deinterlacing to convert the interlaced video signals to progressive scanned video signals.

10. (Original) The system as claimed in Claim 9, wherein said deinterlacer has an access to the frame buffer controller providing field delay for deinterlacing.

11. (Original) The system as claimed in Claim 9, wherein said deinterlacer provides motion information to the de-motion-blur processor.

**Serial Number 10/749,564**

12. (Original) The system as claimed in Claim 1, wherein said pre-frame buffer processor comprises horizontal and vertical scaling down circuits for pixel rate decimating.

13. (Original) The system as claimed in Claim 1, wherein said frame buffer controller comprises a first gate providing an access to the pre-frame-buffer processor and a second gate for providing an access to the scaler and a third gate for providing an access to the de-motion-blur processor, and further comprises an access arbitrator for controlling the gates so that only one gate can write or read data to or from the frame buffer at a time.

14. (Original) The system as claimed in Claim 1, wherein said scaler comprises a main scaling mechanism for converting sample rate for different display resolutions.

15. (Original) The system as claimed in Claim 14, wherein said scaler further comprises a PIP (picture-in-picture) blending unit for combining signals passing the main scaling mechanism and signals bypassing the main scaling mechanism.

16. (Original) The system as claimed in Claim 1, wherein the de-motion-blur processor comprises compression and decompression units for compressing and decompressing the video signals.

17. (Original) The system as claimed in Claim 16, wherein the compression and decompression units using differential PCM to separately process luminance and chrominance components of the video signals.

18. (Original) The system as claimed in Claim 1, wherein the de-motion-blur processor comprises an over drive processing unit for performing over driving for the flat panel display; and a motion noise detector comparing the current and previous video signals, calculating temporal difference value of a pixel of the video signals and determining over driving level of the over drive processing unit according to the difference value.

Serial Number 10/749,564

19. (Original) The system as claimed in Claim 18, wherein the motion and noise detector further receives motion information from the pre-frame-buffer processor and generates a control signal for controlling the over driving level of the over drive processing unit.

20. (Currently Amended) The system as claimed in Claim 18, wherein the motion and noise detector disables the over drive processing unit if the difference value ~~is ignorable~~ indicates a still mode.

21. (Canceled)

22. (Canceled)

23. (Canceled)

24. (Canceled)

25. (Canceled)